REMARKS

Applicants concurrently file herewith a Petition for Extension of Time, and corresponding extension of time fee, for a one-month extension of time.

Claims 1, 2, 9-12, 25-30 and 48-53 are all of the claims presently pending in the application. Applicants have amended claim 1 to define the invention more particularly. Applicants have canceled claims 4-8, 13, 16-24 and 31-47 without prejudice or disclaimer. Applicants have added new claims 48-53 to claim additional features of the invention and to provide varied protection for the claimed invention.

Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1, 2, 9-13 and 25-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu et al. (U.S. Patent No. 6,913,980; hereinafter "Wu") in view of Kubota et al. (U.S. Patent No. 7,094,639; hereinafter "Kubota").

This rejection is respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as defined by claim 1) is directed to a semiconductor device comprising a MIS type field effect transistor.

The transistor includes a silicon substrate, a gate insulating film including a high-dielectric-constant metal oxide film and a silicon containing insulating film lying between the metal oxide film and the silicon substrate, a silicon containing gate electrode formed on the gate insulating film, a gate length of the silicon containing gate electrode being not greater than 1μm, and a sidewall including silicon oxide as a constituting

material, which is formed on each lateral face side of the gate electrode. A silicon nitride film is interposed between the sidewall and at least the lateral face of the gate electrode. The silicon nitride film covers the lateral face of the high-dielectric-constant metal oxide film, and a silicon oxide film underlies the silicon nitride film.

The device of the claimed invention, as exemplarily defined in claim 1, is capable of suppressing, under heating in an oxidizing atmosphere, the permeation and/or penetration of oxidants into the high-dielectric-constant metal oxide film.

II. THE PRIOR ART REJECTION

The Examiner alleges that Kobuta would have been combined with Wu to teach the claimed invention of claims 1, 2, 9-13 and 25-27. Applicants respectfully submit, however, that Kobuta would not have been combined with Wu as alleged by the Examiner.

The claimed invention of exemplary claim 1 recites, *inter alia*, "*a silicon containing gate electrode formed on the gate insulating film, a gate length of said silicon containing gate electrode being not greater than 1 μm*".

This feature of the claimed invention is not taught or suggested by the primary reference Wu. Indeed, the Examiner does not even allege that Wu teaches or suggests this feature of the claimed invention.

Instead, the Examiner alleges that "Kubota et al. (col. 1, lines 18-20) disclose that a gate length of the gate electrode is not greater than 1 μm." (See Office Action dated April 20, 2007 at page 4).

Applicants respectfully submit, however, that the Examiner has failed to establish a *prima facie* case of obviousness.

Indeed, the Examiner has not provided any reason why one of ordinary skill in the art

would have combined this alleged feature of Kubota with the device disclosed in Wu. The Examiner appears to be alleging that the mere presence of the disclosure of a feature in the Kobuta reference is sufficient to find that it would have been obvious to modify the Wu reference based upon this disclosure.

However, the Examiner cannot merely gather a large number of prior art references, which each include some portion of the features recited in the claims, and allege that the mere disclosure of the features in the combination of references is sufficient to allege obviousness of the claimed invention.

Indeed, in order to establish a *prima facie* case of obviousness based on an alleged combination of prior art elements, the Examiner must identify the reason why a person of ordinary skill in the art would have combined the prior art elements in the manner claimed.

Therefore, in this specific instance, the Examiner must identify a reason why a person of ordinary skill in the art would have combined a gate electrode having a gate length not greater than 1 μm with the device of Wu.

Since the Examiner has not provided any reasoning or analysis to support his alleged combination of Kobuta with the device of Wu (with respect to the feature of a gate electrode having a gate length not greater than 1 μm) the Examiner has failed to establish a *prima facie* case of obviousness.

Moreover, notwithstanding the above, Applicants submit that the more the gate length decrease, the greater is the suppression of the operation current (I_{on}) of transistors, particularly in a structure where the gate length is not greater than 1 μm and a high-dielectric-constant material is used for the gate insulating film (see Application at page 2, line 15 through page 3, line 6, and page 11, line 8 through page 12, line 18).

This problem, which is caused by formation of a silicon oxide film or the additional

growth of the silicon oxide film, can be solved by the structure of the claimed invention, because the claimed invention can inhibit the permeation and/or penetration of oxidants into the high-dielectric-constant metal oxide film that constitutes the gate insulating film (see Application at page 12, lines 19-24). In the claimed invention, the silicon nitride film, which is formed to cover the lateral face of the high-dilectric-constant metal oxide film, can prevent oxidants such as oxygen from penetrating into the high-dielectric-constant metal oxide film (e.g., see Application page 20, lines 2-13). The claimed invention is particularly effective when the semiconductor device, including a MISFET, has a gate length that is not greater than 200 nm, and even more effective when the gate length is not greater than 100 nm, because the problem becomes more serious as the gate length decreases (e.g., see Application page 12, line 25 through page 13, line 4; and see exemplary claims 51-53).

Thefore, Applicants submit that Kobuta would not have been combined with Wu as alleged by the Examiner. Accordingly, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. NEW CLAIMS

Applicants have added new claims 48-53 to provide varied protection for the claimed invention and to claim additional features of the invention. These claims are independently patentable because of the novel features recited therein.

Applicants respectfully submit that new claims 48-53 are patentable over any combination of the applied references at least for analogous reasons to those set forth above with respect to claims 1, 2, 9-13 and 25-27.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicants submit that claims 1, 2, 9-12, 25-30 and 48-53, all of the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. Applicants respectfully request the Examiner to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, Applicants respectfully request the Examiner to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

Applicants authorize the Commissioner to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully submitted,

Scott M. Tulino, Esq.
Registration No.: 48,317

Sean M. McGinn, Esq.
Registration No.: 34,386

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MCGINN INTELLECTUAL PROPERTY LAW GROUP, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22182-3817
(703) 761-4100
Customer No. 21254